WHAT IS CLAIMED IS:

1. A flip-flop circuit comprising:

an input terminal;

a clock terminal;

an output terminal;

an input section for receiving a signal input to the input terminal and a clock signal at the clock terminal;

a latch circuit for latching an output of the input section;

a control section for controlling operation of the input section, the control section having a first node; and

an output section for outputting a signal from the output terminal,

wherein the input section has a second node, receives a signal at the first node of the control section as a control signal, outputs a high-level signal from the second node independently of the value of the input signal at the input terminal when the clock signal at the clock terminal is at a low level, and outputs, to the second node, a logic signal depending on the input signal at the input terminal when the clock signal at the clock terminal is at a high level and the control signal from the first node of the control section is at a high level,

the latch circuit has a third node, receives a signal at the second node of the input section, holds the signal at the second node when the clock signal at the clock terminal is at the high level and the control signal from the first node of the control section is at a low level, and outputs, to the third node, a signal which is the logical inverse of the signal at the second node of the input section,

the control section receives the clock signal at the clock terminal and the signal at third node of the latch circuit, outputs a high-level signal to the first node when the clock

signal at the clock terminal is at the low level, and outputs, to the first node, a signal at the same level as that of the signal at the third node of the latch circuit with a delay corresponding to a predetermined delay value when the clock signal at the clock terminal is at the high level, and

the output section receives the signal at the first node of the control section and the signal at the third node of the latch circuit, holds the signal at the output terminal when the signal at the first node of the control section is at the high level and the signal at the third node of the latch circuit is at a low level, outputs, to the output terminal, a logic signal depending on the signal at the first node when the signal at the first node of the control section is at the low level , and outputs a logic signal depending on the signal at the third node when the signal at the third node is at a high level.

2. A flip-flop circuit comprising:

an input terminal;

a clock terminal;

an output terminal;

an input section for receiving a signal input to the input terminal and a clock signal at the clock terminal;

a latch circuit for latching an output of the input section;

a control section for controlling operation of the input section, the control section having a first node; and

an output section for outputting a signal from the output terminal,

wherein the input section has a second node, receives a signal at the first node of the control section as a control signal, outputs a high-level signal from the second node independently of the value of the input signal at the input terminal when the clock signal at

the clock terminal is at a low level, and outputs, to the second node, a logic signal depending on the input signal at the input terminal when the clock signal at the clock terminal is at a high level and the control signal from the first node of the control section is at a high level,

the latch circuit has a third node, receives a signal at the second node of the input section, holds the signal at the second node when the clock signal at the clock terminal is at the high level and the control signal from the first node of the control section is at a low level, and outputs, to the third node, a signal which is the logical inverse of the signal at the second node of the input section,

the control section receives the clock signal at the clock terminal and the signal at third node of the latch circuit, outputs a high-level signal to the first node when the clock signal at the clock terminal is at the low level, and outputs, to the first node, a signal at the same level as that of the signal at the third node of the latch circuit with a delay corresponding to a predetermined delay value when the clock signal at the clock terminal is at the high level, and

the output section holds the signal at the output terminal when a low-level signal is applied to the clock terminal, while outputting, to the output terminal, a logic signal depending on the signal at the second node when a high-level signal is applied to the clock terminal.

3. The flip-flop circuit of claim 1, wherein the control section includes a delay circuit for delaying the control signal to be output to the input section.

4. The flip-flop circuit of claim 2, wherein the control section includes a delay circuit for delaying the control signal to be output to the input section.

5. The flip-flop circuit of claim 1, wherein the latch circuit includes first shut-off means for shutting off a path for current supply to the second node of the input section when the signal at the first node of the control section is at the high level and the signal at the third node of the latch circuit is at the low level.

6. The flip-flop circuit of claim 2, wherein the latch circuit includes first shut-off means for shutting off a path for current supply to the second node of the input section when the signal at the first node of the control section is at the high level and the signal at the third node of the latch circuit is at the low level.

7. The flip-flop circuit of claim 1, wherein the output section includes second shut-off means for shutting off a transmission of a low-level signal, which temporally appears at the first node of the control section, to the output terminal when the signal at the second node of the latch circuit is at a low level.

8. The flip-flop circuit of claim 2, wherein the output section includes second shut-off means for shutting off a transmission of a low-level signal, which temporally appears at the first node of the control section, to the output terminal when the signal at the second node of the latch circuit is at a low level.

9. The flip-flop circuit of claim 1, wherein the output section includes a PMOS transistor having a gate terminal connected to the second node, a source connected to a power supply and a drain connected to the output terminal.

10. The flip-flop circuit of claim 2, wherein the output section includes a PMOS transistor having a gate terminal connected to the second node, a source connected to a power supply and a drain connected to the output terminal.